REMARKS/ARGUMENTS

Claims 1-37 were previously pending in the application. Claims 21-26 and 28-30 are canceled; 1, 4-5, 11-12, 16, 19-20, 27, 33, and 35-36 are amended; and new claims 38-46 are added herein. Assuming the entry of this amendment, claims 1-20, 27, and 31-46 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

In paragraph 1 of the office action, the Examiner stated that the first sentence of the Abstract should be rewritten without using the word "disclosed." In response, the Applicant submits herewith a Substitute Abstract of the Invention that does not use the word "disclosed."

In paragraph 2, the Examiner objected to claims 1-32 and 36-37 because of certain informalities. In response, the Applicant has amended the claims as follows:

- Claims 1 and 16 have been amended to recite "a plurality of multipliers" instead of "a plurality of multiplier."

- Claims 1 and 16 have been amended to recite "a tap weight source" instead of "a top weight source," as suggested by the Examiner.

- Claims 1 and 16 have been amended to recite "each multiplier producing an output corresponding to a product of the first and second inputs" instead of "each multiplier producing an output that is a product of inputs thereto." In addition to addressing the antecedence problem cited by the Examiner, this amendment clarifies that the output produced by each multiplier need not be the result of an actual multiplication operation *per se*, as described on page 5, lines 13-17, of the specification.

- Claims 1 and 16 have been amended to recite "the tap weight shifter capable of shifting tap weights" instead of "the tap weight shifter capable of circularly shifting tap weights." This amendment clarifies that shifting of the tap weights can be, but need not always be circular.

- Claims 4 and 19 have been amended to clarify the claim language and to refer to the antecedent recitation of "tap weights."

- Claim 11 has been amended as suggested by the Examiner.

- Claims 12 and 27 have been amended to refer to the antecedent recitations of "tap weight source" and "tap weights."

- Claim 33 has been amended to add a semi-colon at the end of step c.

- Claim 36 has been amended as suggested by the Examiner.

The Applicant submits that none of these aforementioned amendments have been made to overcome any prior art rejections.

In paragraph 4, the Examiner rejected claim 5 under 35 U.S.C. 112, second paragraph, as being indefinite. In response, the Applicant has amended claim 5 to clarify that "the tap weights received by

the tap weight shifter are more than one bit wide" and that "the tap weights have a bit width that is no greater than a bit width of stages of the shift registers." Claim 20 has been similarly amended.

In paragraph 6, the Examiner rejected claims 1, 4-5, 12, 16, 19-20, 27, 33, and 35-36 under 35 U.S.C. 102(e) as being anticipated by Zhou. In paragraph 8, the Examiner rejected claims 2-3, 17-18, 34, and 37 under 35 U.S.C. 103(a) as being unpatentable over Zhou in view of Nishida. In paragraph 9, the Examiner rejected claims 6-11, 21-26, and 32 under 103(a) as being unpatentable over Zhou in view of Nishida and further in view of Schilling. In paragraph 10, the Examiner rejected claims 13-14, 28-29, and 31 under 103(a) as being unpatentable over Zhou in view of Nishida and further in view of Black. In paragraph 11, the Examiner rejected claims 15 and 30 under 103(a) as being unpatentable over Zhou in view of Nishida and further in view of Gronemeyer. For the following reasons, the Applicant submits that all of the now-pending claims are allowable over the cited references.

Claims 1 and 16

Claims 1 and 16 have been further amended to clarify that two or more sum outputs are generated between consecutive shiftings of new data into the shift registers. This feature relates to a digital filter that generates two or more different sums for each set of data stored in the shift registers.

Zhou teaches, in Fig. 3 and on column 3, line 28, to column 4, line 24, a matched filter that has two data register sequences (R11 to R1n and R21 to R2n). The output of each data register R1i and the output of the corresponding data register R2i are input to a corresponding selector SELi, which selectively outputs one of those two data register outputs to a corresponding exclusive-or-gate XORi, which combines the selected data register output with a corresponding bit of the PN code sequence stored in shift register SREG. The outputs from the n XOR gates are then combined in a current addition circuit ADD to generate the analog output signal A_{out}.

In Zhou, an analog data signal data Ain is digitized and then double-sampled when loaded into the two data register sequences, where "one and only one of the data registers holds the output of the A/D converter at one time." Significantly, the two data register sequences in Zhou are not shift registers. In particular and for example, the data from register R11 is never shifted into register R12, or vice versa. Rather, after a datum is loaded into the last register R1n, the next datum for that data register sequence is loaded into the first register R11 (overwriting the previously stored datum value), the following datum for that data register is loaded into the second register R12, and so on. As such, at any given time, the "oldest" datum can be stored in any of the data registers (e.g., R1j) with the "newest" datum stored in the previous data register in the sequence (e.g., R1 j-1), where "j-1" is n, for the particular case when "j" is 1.

To match this data-loading cycle, the PN code sequence in Zhou is circularly shifted in shift register SREG to ensure that the proper PN code bits are combined at the XOR gates with the corresponding data values in the selected data registers. According to Zhou, the clock CLKS, which controls the cycling of the PN code sequence in shift register SREG, is synchronous with the clocks CLK1 and CLK2, which control the loading of data into the two data register sequences, "such that the PN code sequence is shifted and circulated corresponding to the data input to the data registers from the A/D converter." Thus, in Zhou, there is exactly one value of the analog output signal A_{out} generated for each set of data stored in the selected data registers.

To summarize, the teachings in Zhou differ from the invention of claims 1 and 16 in (at least) the following way. In claims 1 and 16, two or more sum outputs are generated between consecutive shiftings of new data into the shift registers, while, in Zhou, no more than one output value is generated between consecutive storings of new data into the data register sequences.

None of the other cited references of record teach the features of claims 1 and 16 that are missing from Zhou.

For all these reasons, the Applicant submits that claims 1 and 16 are allowable over the cited references. Since claims 2-15 and 17-32 depend variously from claims 1 and 16, it is further submitted that those claims are also allowable over the cited references.

Claim 33

According to the method of currently amended claim 33, (a) digital data is shifted into first and second multiple stage shift registers, (b) an output from each stage of the first and second multiple stage shift registers is multiplied by an associated, respective tap weight to produce a plurality of products; (c) the plurality of products are combined to form a sum, (d) the tap weights are circularly shifted, and (e) steps (b) and (c) are repeated at least once before step (a) is repeated. In light of the previous discussion, the invention of claim 33 differs from the teachings in Zhou for (at least) the following reasons.

First of all, in Zhou, each selector SELi selects one datum from each pair of corresponding data registers R1i and R2i to be applied to the corresponding XOR gate XORi. Thus, Zhou does not teach an output from each stage of first and second shift registers being multiplied by an associated, respective tap weight.

Secondly, in Zhou, at most a single output is generated for each loading of new data into the shift register sequences. Thus, Zhou does not teach the generation of a second sum before shifting new data into first and second shift registers.

None of the other cited references of record teach these features of claim 33 that are missing from Zhou.

For all these reasons, the Applicant submits that claim 33 is allowable over the cited references. Since claim 34 depends from claim 33, it is further submitted that claim 34 is also allowable over the cited references.

Claim 35

According to the method of currently amended claim 35, (a) data is shifted into N multiple stage shift registers, each of the N multiple stage shift registers having at least L stages, N and L being integers, N being at least 2, (b) an output from each of the at least L stages of the N multiple stage shift registers is multiplied by a corresponding tap weight to produce a plurality of products, (c) the plurality of products are combined to form a sum, (d) the tap weights are circularly shifted, (e) steps b, c, and d are repeated N-2 times before step a is repeated, and (f) steps b and c are repeated again before step a is repeated. In light of the earlier discussion, the invention of claim 35 differs from the teachings in Zhou for (at least) the following reasons.

First of all, in Zhou, each selector SELi selects one datum from each pair of corresponding data registers R1i and R2i to be applied to the corresponding XOR gate XORi. Thus, Zhou does not teach an output from each stage of first and second shift registers being multiplied by a corresponding tap weight.

Secondly, in Zhou, at most a single output is generated for each loading of new data into the shift register sequences. Thus, Zhou does not teach the generation of a second sum before shifting new data into N shift registers.

None of the other cited references of record teach these features of claim 35 that are missing from Zhou.

For all these reasons, the Applicant submits that claim 35 is allowable over the cited references. Since claims 36-37 depends from claim 35, it is further submitted that those claims are also allowable over the cited references.

Claims 38 and 46

According to new claims 38 and 46, the digital filter has *N* multiple-stage shift registers, a tap changer, a plurality of multiplying elements, and an adder, where the digital filter can generate two or more sums for each set of data stored in the shift registers. For at least some of the same reasons provided earlier, the Applicant submits that claims 38 and 46 are allowable over the cited references. Since claims 39-45 depend variously from claim 38, it is further submitted that those claims are also allowable over the cited references.

In view of the foregoing, the Applicant submits that the rejections of claims under Sections 102(e) and 103(a) have been overcome.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

Date: 7/13/04

Steve Mendelsohn
Registration No. 35,951
Attorney for Applicant
(215) 557-6657 (phone)
(215) 557-8477 (fax)

Customer No. 22186
Mendelsohn & Associates, P.C.
1515 Market Street, Suite 715
Philadelphia, Pennsylvania 19102

SUBSTITUTE ABSTRACT OF THE INVENTION

A digital filter or a receiver including a digital filter having at least two multiple stage shift registers. A plurality of multipliers corresponding in number to the number of stages in the at least two multiple stage shift registers receive as a first input an output from a corresponding stage of the at least two multiple stage shift registers. A tap weight shifter is coupled to a tap weight source to receive tap weights. The tap weight shifter is coupled to provide a second input to each multiplier. Each multiplier produces an output that is the product of inputs thereto. An adder sums the multiplier outputs to provide a sum output. The tap weight shifter then circularly shifts the tap weights and another multiply-add operation occurs. Several shift/multiply/add cycles may occur before data is again shifted into the at least two multiple stage shift registers, and another multiply-add operation occurs.